

ESTEL ELEKTROONIKA
ESTONIAMarch
2005**Series**
TFI473-1600**High Frequency Inverter grade**
Capsule Thyristor
Type TFI473-1600Low switching losses
Distributed amplified gate for high di/dt

Preliminary data

Maximum mean on-state current						I_{TAV}	1600 A
Maximum repetitive peak off-state and reverse voltage						U_{DRM}	3400 ÷ 4400 V
Turn-off time						U_{RRM}	
						t_q	125; 160 μs
U _{DRM} , U _{RRM} , V	3400	3600	3800	4000	4200	4400	
Voltage code	34	36	38	40	42	44	
T _{vj} , °C	- 60 ÷ 125						

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	TFI473-1600	Conditions	
I _{TAV}	Mean on-state current	A	1600 2190	T _c =80 °C, T _c =55 °C, 180° half-sine wave, 50 Hz	
I _{TRMS}	RMS on-state current	A	2512	T _c =80 °C	
I _{TSM}	Surge on-state current	kA	30,0 33,0	T _{vj} =125°C T _{vj} =25°C	tp=10 ms U _R =0
I ² t	Limiting load integral	kA ² s	4500 5445	T _{vj} =125°C T _{vj} =25°C	
U _{DRM} , U _{RRM}	Repetitive peak off-state and reverse voltage	V	3400÷4400	T _{j min} ≤T _{vj} ≤T _{jM} 180° half-sine wave, 50 Hz Gate open	
U _{DSM} , U _{RSM}	Non-repetitive peak off-state and reverse voltage	V	3500÷4500	T _{j min} ≤T _{vj} ≤T _{jM} 180° half-sine wave tp=10 ms, Single pulse Gate open	
(di _T /dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/μs	1600 800	T _{vj} =125°C ; U _D =0,67 U _{DRM} , Gate pulse : 10V, 5 Ω, 1μs rise time, 10 μs	
U _{RGM}	Peak reverse gate voltage	V	5	T _{j min} ≤T _{vj} ≤T _{jM}	
T _{stg}	Storage temperature	°C	-60÷80		
T _{vj}	Junction temperature	°C	-60÷125		

CHARACTERISTICS

U _{TM}	Peak on-state voltage	V	3,0	T _{vj} =25°C, I _{TM} =3,14 I _{TAV}
U _{T(TO)}	Threshold voltage	V	1,1	T _{vj} =125°C
R _T	On-state slope resistance	mΩ	0,25	1,57 I _{TAV} < I _T <4,71 I _{TAV}
I _{DRM} I _{RRM}	Repetitive peak off-state and reverse current	mA	200 200	T _{vj} =125°C, U _D =U _{DRM} U _R =U _{RRM}

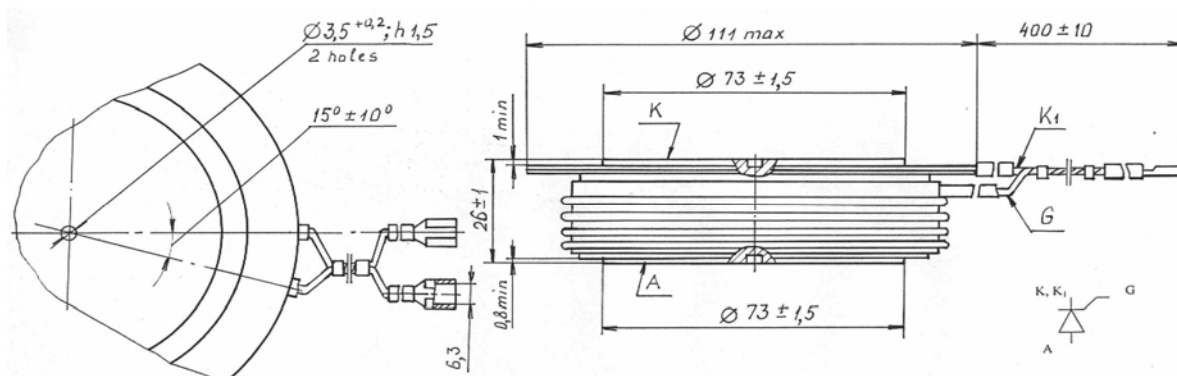
CHARACTERISTICS

Symbols and parameters		Units	TFI473-1600	Conditions
I_L	Latching current	A	15	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$ Gate pulse : 10V, 5 Ω , 1 μs rise time, 10 μs
I_H	Holding current	A	1,0	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$, Gate open
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	$T_{vj}=25^{\circ}\text{C}$, $T_{vj}=-60^{\circ}\text{C}$
I_{GT}	Gate trigger direct current	A	0,35 0,85	$T_{vj}=25^{\circ}\text{C}$, $T_{vj}=-60^{\circ}\text{C}$
U_{GD}	Gate non-trigger direct voltage	V	0,25	$T_{vj}=125^{\circ}\text{C}, U_D = 0,67 U_{DRM}$
I_{GD}	Gate non-trigger direct current	mA	10	Direct gate current
t_{gd}	Delay time	μs	2,5	$T_{vj}=25^{\circ}\text{C}, U_D=500\text{V}$ $I_{TM} = 1600 \text{ A}$
t_{gt}	Turn-on time	μs	4,0	Gate pulse : 10V, 5 Ω , 1 μs rise time, 10 μs
t_q	Turn-off time	μs	125; 160 160; 200	$T_{vj}=125^{\circ}\text{C}, I_{TM}=1600 \text{ A}$ $di_R/dt = 10 \text{ A}/\mu\text{s}, U_R=100\text{V}$ $U_D = 0,67 U_{DRM}$ $du_D/dt=50 \text{ V}/\mu\text{s}$ $du_D/dt=200 \text{ V}/\mu\text{s}$
Q_{rr}	Recovered charge	μC	3300	
t_{rr}	Reverse recovery time	μs	14	$T_{vj}=125^{\circ}\text{C}, I_{TM}=1600 \text{ A}$
I_{rrM}	Peak reverse recovery current	A	470	$di_R/dt = 50 \text{ A}/\mu\text{s}, U_R=100\text{V}$
$(du_D/dt)_{crit}$	Critical rate of rise of off-state voltage	$\text{V}/\mu\text{s}$	500 1000	$T_{vj}=125^{\circ}\text{C}, U_D = 0,67 U_{DRM}$ Gate open
R_{thjc}	Thermal resistance junction to case	$^{\circ}\text{C}/\text{W}$	0,013	Direct current, double side cooled

ORDERING

	TFI	473	1600	40	7	T2	1	
	1	2	3	4	5	6	7	

1. Fast thyristor with interdigitated gate structure.
2. Design version.
3. Mean on-state current, A.
4. Voltage code (40=4000V).
5. Critical rate of rise of off-state voltage ($6 \geq 500 \text{ V}/\mu\text{s}$, $7 \geq 1000 \text{ V}/\mu\text{s}$)
6. Group of turn-off time ($du_D/dt=50 \text{ V}/\mu\text{s}$, $T_2 \leq 160 \mu\text{s}$, $X_2 \leq 125\mu\text{s}$)
7. Group of turn-on time ($1 \leq 4 \mu\text{s}$)



Mounting force : 36 ÷ 46 kN
Weight : 1200 grams